Application of High Power Silicon Carbide Transistors at Radar Frequencies

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ABSTRACT

Silicon carbide (SiC) is an emerging semiconductor material which has been widely predicted to allow greatly improved transistor performance over common semiconductors such as silicon and gallium arsenide. This paper describes the characteristics of recently fabricated devices in silicon carbide, and the first application of silicon carbide transistors in high power pulsed amplifiers at radar frequencies.

INTRODUCTION

Silicon carbide has been previously predicted to have superior performance relative to silicon and GaAs for high power applications [1][2]. The key qualities of silicon carbide which are notable are its high voltage breakdown (10X that of silicon or GaAs), thermal conductivity (10X that of GaAs), superior saturated carrier velocity, and temperature range. These physical advantages are ideal for design of high frequency power devices, and point to large potential improvements in achievable device power and power density.

The inherent high voltage advantage of SiC enhances one end of the device load line, and the high carrier velocity facilitates high device current density, which is the other end of a superior high power load line. The exceptional electrical power density thus available is accessible in practical devices because of the thermal characteristics of the material. The high thermal conductivity of SiC provides superior conduction of the waste heat generated by the higher power density, and the high temperature capability of the material allows the use of unusually high temperature gradients.

Whereas incremental power improvements are still being achieved in Si and GaAs transistors, by use of a radically new semiconductor system, large improvements in power are predictable, on the order of four to ten times greater power and power density. The practical upper frequency limit for SiC amplifiers will be shown here to reach at least S-Band.

Silicon carbide has some well known drawbacks, such as relatively low mobility, lack of high quality materials, and difficulty in device fabrication processing. Single crystal wafers are only recently commercially available, and they still are small (about 4 cm diameter), with defect densities which are orders of magnitude worse than either commercial silicon or GaAs. These limitations on quality of basic materials have hitherto discouraged practical experimentation or development of large power devices.

The results reported here illustrate that the historical difficulties with silicon carbide can now be managed, and that many of the important theoretical predictions for improved device and circuit performance have been reached. In particular, silicon carbide transistors have been fabricated with

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power output of over 450 watts at 600 MHz, and a multi-transistor module has been developed at the 1 kW level. At S-Band, demonstrated gain and power density results exceed that which is available with silicon technology.

LARGE DEMONSTRATION DEVICE AND CHARACTERISTICS

The static induction transistor (SIT) is a device structure which can be fabricated in SiC, and is also known in more common semiconductors[3][4]. Commercially, the SIT is sometimes referred to as a "Solid State Triode", because its curves are non-saturating like those of a triode vacuum tube. In silicon, the SIT usually has higher voltage breakdown than comparable bipolar devices, and RF power capability, into the low GHz range, which rivals that of bipolar transistors. The SIT geometry was chosen for experimentation with silicon carbide because it is a majority carrier device and tolerates the very low hole mobility of SiC.

Interdigitated SIT cells having 1.5 cm total gate periphery were fabricated in SiC at the Northrop Grumman Science and Technology Center[5]. The cells were fabricated on currently available silicon carbide wafers which have defect densities in the 50 to 200 per cm^2 range. Because of these relatively high wafer defect levels, many cells were defective, although clusters of good cells were readily found by on-wafer voltage probing. A total of 60 cells, contained on three separate die, were mounted into a standard 0.4 inch power transistor package. 23 of the 60 cells were found to pass a 250 V breakdown test and were subsequently wired in parallel for 34.5 cm total periphery. The packaged device contains no internal matching components other than paralleled wire bonds, and is illustrated in figure 1. The packaged impedance levels at 600 MHz were found to have magnitudes of approximately 2 ohms on the input, and 4.1 ohms for an optimum drain circuit load. These relatively high values of unmatched impedances reflect the high voltage swings at the cells, which are about 2.5 times higher than on similar structures available in silicon, and low parasitic capacitances, due to the exceptionally small physical size of the active cells.

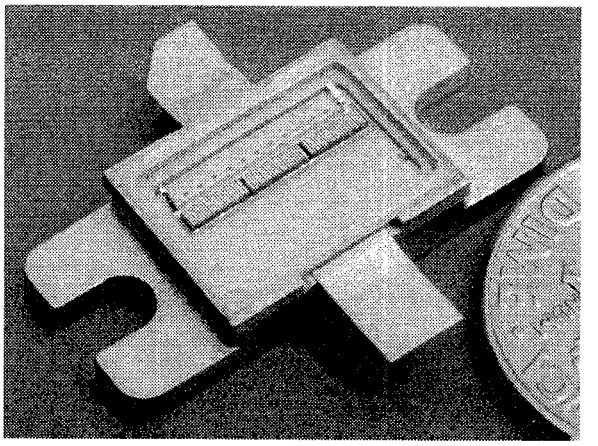

Figure 1. Packaged SiC Transistor

The unmatched device was operated in a microstrip circuit at 90 volts drain bias at 600 MHz with the performance shown in figure 2. The power output density of the paralleled cells is 165 kw/in^2. This value is substantially higher than the practical limit seen in silicon devices of 78 $Watts/in^2$, and is a direct fallout of the unique physical characteristics of SiC. Projected device power with 50% yield on the cells would be 580 watts, and 1175 watts when material quality allows close to 100% yield on the selected die.

The power transfer characteristic in Figure 2 shows good linearity of the SiC SIT structure in common source, class AB operation.

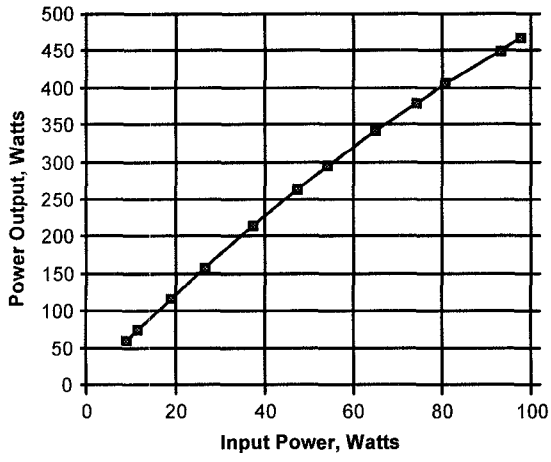

Figure 2. 34.5 cm SiC SIT at 600 MHz

DEMONSTRATION MODULE DESIGN

Five multi-cell SITs were fabricated in the 0.4 inch packages. Operable cells were identified by means of a 250 volt BV_{DS} test and subsequently bonded in parallel to form a complete multi-cell transistor. The finished devices showed total peripheries of 24, 24, 24, 22.5, and 22.5 cm. As was the case in the larger demonstration device, internal matching was not necessary for 600 MHz operation, owing to the high operating impedance levels in SiC devices. The devices were assembled into a module as shown in figure 3. The module measures 5 x 8 x 1.5 inches and is constructed with soft Teflon-ceramic substrate with air cooling fins bonded to the bottom. The module combines four devices in an output stage, with one of the 22.5 cm devices used as an additional driver stage.

Microstrip tuning was sufficient to match the devices to the 50 ohm level, and the four output devices combined well, even though one device was slightly smaller in periphery than the others. 4:1 combining and splitting was done with a combination of Wilkinson and Wireline couplers. The module was operated at 90 volts drain bias on all devices, with the performance shown in figure 4.

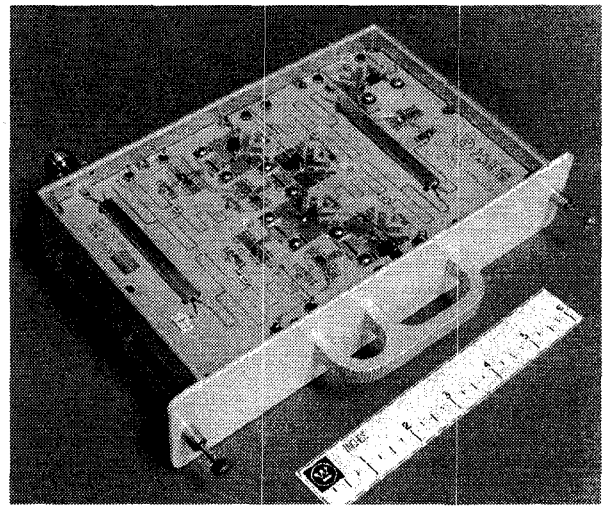

Figure 3. One Kilowatt SiC Module

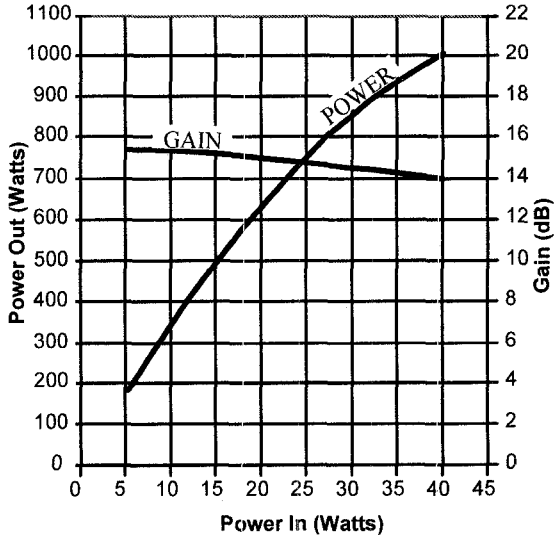

Figure 4. Silicon Carbide Module at 600 MHz

HIGH FREQUENCY TRANSISTOR APPLICATION

An improved silicon carbide SIT design was fabricated into 1 cm cells and mounted into a standard 0.25 inch hermetic pill package, which is commonly used to house unmatched silicon bi-polar transistors up to

5W at S-Band. Figure 5 shows an array of 11 cells in the package, with 3 selected cells bonded in parallel. Each cell has 1 cm total periphery. The unmatched, 3-cm silicon carbide device was built into a microstrip amplifier and operated at 80 volts drain bias. Figure 6 shows that over 36 watts is obtained at 3 GHz for 55μs pulses, with 9.5 dB overall gain and 42% power added efficiency. This single transistor amplifier exhibits four times the practical power density of commercial silicon technology, at impedance levels which do not require internal package matching components.

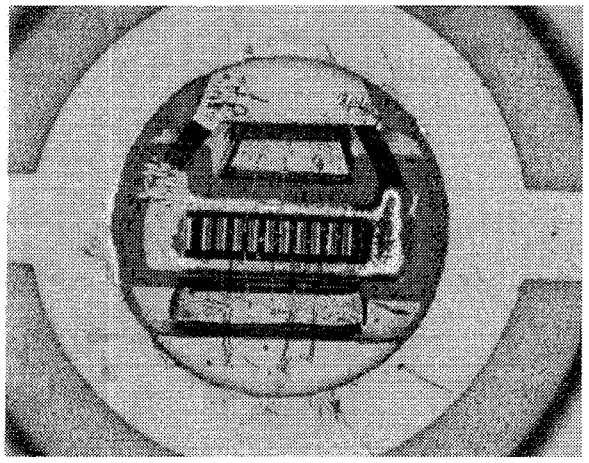

Figure 5. SiC SIT in Pill Pkg.

CONCLUSIONS

High frequency transistors in silicon carbide are available in experimental quantities at power levels over 200 Watts, using current material quality and processing yields. The SIT structure in silicon carbide provides very high power density and combines well at the cell level, and also between packaged devices which are similar in size to each other. The power density of devices fabricated in SiC is several times higher than is practical in either Si or GaAs devices, and leads to much higher single device power levels. The high voltage levels in silicon carbide lead to impedance levels which are more manageable than those which may be obtained using silicon or GaAs. The high operating voltage with SiC devices will require correspondingly lower currents for a given power, which has benefit to integration of high power arrays.

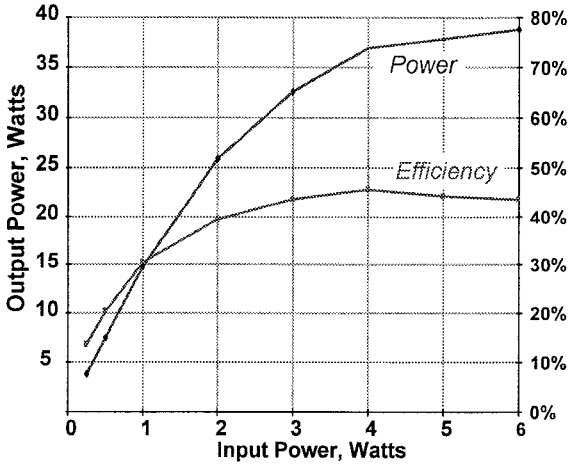

Figure 6. Single Stage SiC Common Gate Amplifier at 3 GHz

ACKNOWLEDGMENTS

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